

IN THE CLAIMS:

Please amend the following claims:

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1           2. (Amended) A semiconductor integrated circuit  
2 according to claim 1, wherein said first logic gate  
3 includes an MIS transistor to which a substrate bias is  
4 applied in a reverse direction by a substrate potential,  
5 and said second logic gate includes an MIS transistor to  
6 which a substrate bias is applied in a forward direction by  
7 said substrate potential.

1           3. (Amended) A semiconductor integrated circuit  
2 according to claim 1, wherein said first logic gate  
3 includes a p-channel type MIS transistor and an n-channel  
4 type MIS transistor to which substrate biases are applied  
5 in a reverse direction by respective substrate potentials,  
6 and said second logic gate includes a p-channel type MIS  
7 transistor and an n-channel type MIS transistor to which  
8 substrate biases are applied in a forward direction by the  
9 respective substrate potentials.

1           4. (Amended) A semiconductor integrated circuit  
2 according to claim 1, wherein said first logic gate

3 includes a p-channel type MIS transistor to which a  
4 substrate bias is applied in a reverse direction by a  
5 substrate potential, and said second logic gate includes a  
6 p-channel type MIS transistor to which a substrate bias is  
7 applied in a forward direction by said substrate potential.

1 5. (Amended) A semiconductor integrated circuit  
2 according to claim 1, wherein said first logic gate  
3 includes a p-channel type MIS transistor and an n-channel  
4 type MIS transistor to which substrate biases are applied  
5 in a reverse direction by respective substrate potentials.

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1 8. (Twice Amended) A semiconductor integrated circuit  
2 according to claim 6, wherein said first logic gate  
3 includes an MIS transistor to which a substrate bias is  
4 applied in a reverse direction by a potential in the well  
5 region thereof, and said second logic gate includes an MIS  
6 transistor to which a substrate bias is applied in a  
7 forward direction by a potential in the well region  
8 thereof.

1 9. (Twice Amended) A semiconductor integrated circuit  
2 according to claim 6, wherein said first logic gate

3 includes a p-channel type MIS transistor and an n-channel  
4 type MIS transistor to which substrate biases are applied  
5 in a reverse direction by respective potentials of the well  
6 regions thereof, and said second logic gate includes a p-  
7 channel type MIS transistor and an n-channel type MIS  
8 transistor to which substrate biases are applied in a  
9 forward direction by respective potentials of the well  
10 regions thereof.

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1 10. (Twice Amended) A semiconductor integrated  
2 circuit according to claim 6, wherein said first logic gate  
3 includes a p-channel type MIS transistor to which a  
4 substrate bias is applied in a reverse direction by a  
5 potential of the well region thereof, and said second logic  
6 gate includes a p-channel type MIS transistor to which a  
7 substrate bias is applied in a forward direction by a  
8 potential in the well region thereof.

1 11. (Twice Amended) A semiconductor integrated  
2 circuit according to claim 6, wherein said first logic gate  
3 includes a p-channel type MIS transistor and an n-channel  
4 type MIS transistor to which substrate biases are applied

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5 in a reverse direction by respective potentials in the well  
6 regions thereof.

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1 13. (Amended) A semiconductor integrated circuit  
2 according to claim 12, wherein said first potential pair  
3 includes a first high potential and a first low potential,  
4 said second potential pair includes a second high potential  
5 higher than said first high potential and a second low  
6 potential lower than said first low potential, and said  
7 substrate potential is one of a high potential side  
8 substrate potential between said first and second high  
9 potentials and a low potential side substrate potential  
10 between said first and second low potentials.

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1 17. (Amended) A semiconductor integrated circuit  
2 according to claim 16, wherein  
3 said first potential line pair includes a first high  
4 potential line and a first low potential line,  
5 said second potential line pair includes a second high  
6 potential line having a potential higher than that of said  
7 first high potential line and a second low potential line  
8 having a potential lower than said first low potential  
9 line, and

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10        said substrate potential line is one of a high  
11        potential side substrate potential line having a potential  
12        between the potential of said first high potential line and  
13        the potential of said second high potential line, and a low  
14        potential side substrate potential line having a potential  
15        between the potential of said first low potential line and  
16        the potential of said second low potential line.

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1        19. (Amended) A semiconductor integrated circuit  
2        according to claim 16, wherein said first potential line  
3        pair includes a first high potential line and a first low  
4        potential line,  
5        said second potential line pair includes said first  
6        low potential line and a second high potential line having  
7        a potential higher than that of the first high potential  
8        line, and  
9        said substrate potential line is one of a high  
10        potential side substrate potential line having a potential  
11        between the potential of said first high potential line and  
12        the potential of the second high potential line, and a low  
13        potential side substrate potential line having a potential  
14        higher than the potential of said first low potential line.

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1           21. (Amended) A semiconductor integrated circuit  
2 according to claim 20, wherein said first logic gate  
3 includes an MIS transistor to which a substrate bias is  
4 applied in a reverse direction by a substrate potential,  
5 and

6           said second logic gate includes an MIS transistor to  
7 which a substrate bias is applied in a forward direction by  
8 said substrate potential.

1           22. (Amended) A semiconductor integrated circuit  
2 according to claim 20, wherein said first logic gate  
3 includes a p-channel type MIS transistor and an n-channel  
4 type MIS transistor to which substrate biases are applied  
5 in a reverse direction by respective substrate potentials,  
6 and  
7           said second logic gate includes a p-channel type MIS  
8 transistor and an n-channel type MIS transistor to which  
9 substrate biases are applied in a forward direction by the  
10 respective substrate potentials.

1           23. (Amended) A semiconductor integrated circuit  
2 according to claim 20, wherein said first logic gate  
3 includes a p-channel type MIS transistor to which substrate

4 bias is applied in a reverse direction by a substrate  
5 potential, and

6 said second logic gate includes a p-channel type MIS  
7 transistor to which a substrate bias is applied in a  
8 forward direction by said substrate potential.

24. (Amended) A semiconductor integrated circuit  
according to claim 20, wherein said first logic gate  
includes a p-channel type MIS transistor and an n-channel  
type MIS transistor to which substrate biases are applied  
in a reverse direction by respective substrate potentials.

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37. (Twice Amended) A design data recording medium on  
which design data for forming an integrated circuit on a  
semiconductor chip is recorded so as to be readable by a  
computer, the design data comprising:  
first mask pattern data for determining a figure  
pattern for forming a well region on which a plurality of  
logic gates is formed;  
second mask pattern data for determining a figure  
pattern for forming a first line pair, a second line pair  
and a third line pair on said well region; and

11 third mask pattern data for determining a figure  
12 pattern for forming a plurality of connectors,  
13 wherein a first group of said connectors connects said  
14 first line pair and portions of said well region,  
15 wherein a second group of said connectors connects  
16 said second line pair and a first group of said logic gates  
17 for supplying a first potential difference to said first  
18 group of logic gates in an active operation mode, and  
19 wherein a third group of said connectors connects said  
20 third line pair and a second group of said logic gates for  
21 supplying a second potential difference which is larger  
22 than said first potential difference to said second group  
23 of logic gates in said active operation mode.

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1 39. (Amended) A semiconductor integrated circuit  
2 according to claim 7, wherein said first logic gate  
3 includes an MIS transistor to which a substrate bias is  
4 applied in a reverse direction by a potential in the well  
5 region thereof, and said second logic gate includes an MIS  
6 transistor to which a substrate bias is applied in a  
7 forward direction by a potential in the well region  
8 thereof.



1           40. (Amended) A semiconductor integrated circuit  
2 according to claim 7, wherein said first logic gate  
3 includes a p-channel type MIS transistor and an n-channel  
4 type MIS transistor to which substrate biases are applied  
5 in a reverse direction by respective potentials of the well  
6 regions thereof, and said second logic gate includes a p-  
7 channel type MIS transistor and an n-channel type MIS  
8 transistor to which substrate biases are applied in a  
9 forward direction by respective potentials of the well  
10 regions thereof.

1           41. (Amended) A semiconductor integrated circuit  
2 according to claim 7, wherein said first logic gate  
3 includes a p-channel type MIS transistor to which a  
4 substrate bias is applied in a reverse direction by a  
5 potential of the well region thereof, and said second logic  
6 gate includes a p-channel type MIS transistor to which a  
7 substrate bias is applied in a forward direction by a  
8 potential in the well region thereof.

1           42. (Amended) A semiconductor integrated circuit  
2 according to claim 7, wherein said first logic gate  
3 includes a p-channel type MIS transistor and an n-channel

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4 type MIS transistor to which substrate biases are applied  
5 in a reverse direction by respective potentials in the well  
6 regions thereof.

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Please add the following claims:

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1 43. (New) A semiconductor integrated circuit  
2 according to claim 1, wherein said first and second logic  
3 gates are supplied with said first and second potential  
4 pairs, respectively, as power sources in a standby mode.

1 44. (New) A semiconductor integrated circuit  
2 according to claim 6, wherein said first and second logic  
3 gates are supplied with said first and second potential  
4 pairs, respectively, as power sources in a standby mode.

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1 45. (New) A semiconductor integrated circuit  
2 according to claim 7, wherein said first and second logic  
3 gates are supplied with said first and second potential  
4 pairs, respectively, as power sources in a standby mode.

1 46. (New) A semiconductor integrated circuit  
2 according to claim 12, wherein said first and second logic

3 gates are supplied with said first and second potential  
4 pairs, respectively, as power sources in a standby mode.

1 47. (New) A semiconductor integrated circuit  
2 according to claim 16, wherein said first and second logic  
3 gates are connected to said first and second potential line  
4 pairs, respectively, in a standby mode.

1 48. (New) A semiconductor integrated circuit  
2 according to claim 20, wherein said first and second logic  
3 gates are supplied with said first and second potential  
4 pairs, respectively, as power sources in a standby mode.

1 49. (New) A semiconductor integrated circuit  
2 according to claim 37, wherein said first and second groups  
3 of logic gates are supplied from said second and third line  
4 pairs, respectively, in a standby mode.

1 50. (New) A semiconductor integrated circuit  
2 according to claim 38, wherein said first and second logic  
3 gates are supplied from said first and second potential  
4 line pairs, respectively, in a standby mode.

1 51. (New) A semiconductor integrated circuit  
2 comprising:

3 a first logic gat which is supplied with a first  
4 potential difference as a sole operation power source from  
5 a first line pair; and

6 a second logic gate which is supplied with a second  
7 potential difference as a sole operation power source from  
8 a second line pair,

9 wherein said first potential difference is smaller  
10 than said second potential difference, and

11 wherein a substrate potential of MIS transistors is  
12 commonly used by said first and second logic gates.

1 52. (New) A semiconductor integrated circuit  
2 comprising:

3 a first logic gate which is supplied with a first  
4 potential difference as a sole operation power source from  
5 a first line pair; and

6 a second logic gate which is supplied with a second  
7 potential difference as a sole operation power source from  
8 a second line pair,

9 wherein said first potential difference is smaller  
10 than said second potential difference, and

11 wherein said first and second logic gates have MIS  
12 transistors, and a well region in which an MIS transistor

13 of said first logic gate is formed and a well region in  
14 which an MIS transistor of said second logic gate is formed  
15 are made common for each conduction type.

1 53. (New) A semiconductor integrated circuit

2 comprising:

3 a first logic gate which is supplied with a first  
4 potential difference as a sole operation power source from  
5 a first line pair; and

6 a second logic gate which is supplied with a second  
7 potential difference as a sole operation power source from  
8 a second line pair,

9 wherein said first potential difference is smaller  
10 than said second potential difference, and

11 wherein said first and second logic gates have MIS  
12 transistors, and a well region in which an MIS transistor  
13 of said first logic gate is formed and a well region in  
14 which an MIS transistor of said second logic gate is formed  
15 are electrically connected for each conduction type.

1 54. (New) A semiconductor integrated circuit

2 comprising:

3 a first logic gate which is supplied with a first  
4 potential difference as a sole operation power source from

5 a first line pair of a high potential and a low potential;  
6 and

7 a second logic gate which is supplied with a second  
8 potential difference as a sole operation power source from  
9 a second line pair of a high potential and a low potential,  
10 wherein said first potential difference is smaller  
11 than said second potential difference,

12 wherein a substrate potential of an MIS transistor in  
13 said first logic gate and that of an MIS transistor in said  
14 second logic gate are common to each other, and

15 at least said first logic gate includes an MIS  
16 transistor to which a substrate bias is applied in a  
17 reverse direction by said substrate potential.

1 55. (New) A semiconductor integrated circuit  
2 comprising:

3 a first logic gate connected to receive a first  
4 potential difference as a sole operation power source from  
5 a first pair of a high potential line and a low potential  
6 line; and

7 a second logic gate connected to receive a second  
8 potential difference as a sole operation power source from  
9 a second pair of a high potential line and a low potential

10 line,

11 wherein said first potential difference is smaller  
12 than said second potential difference,

13 wherein a substrate potential line is commonly used  
14 for supplying a substrate potential to an MIS transistor of  
15 said first logic gate and for supplying a substrate  
16 potential to an MIS transistor of said second logic gate,  
17 and

18 at least said first logic gate includes an MIS  
19 transistor to which a substrate bias is applied in a  
20 reverse direction by said substrate potential.

1 56. (New) A semiconductor integrated circuit having a  
2 circuit region in which a number of logic gates each having  
3 an MIS transistor are arranged on a semiconductor  
4 substrate,

5 wherein said circuit region has a well region  
6 including portions shared by a substrate potential for each  
7 conduction type of MIS transistor,

8 a first logic gate is supplied with a first potential  
9 difference as a sole operation power source from a first  
10 line pair,

11 a second logic gate is supplied with a second

12 potential difference as a sole operation power source from  
13 a second line pair,

14 said first logic gate and said second logic gate are  
15 formed in said well region,

16 said first potential difference is smaller than said  
17 second,

18 in said well region, a p-type well portion in which an  
19 n-channel type MIS transistor is formed and an n-type well  
20 portion in which a p-channel type MIS transistor is formed  
21 are adjacent to each other, and

22 metal lines for supplying said first potential  
23 difference, said second potential difference, and a  
24 substrate potential are arranged on said well region.

1 57. (New) A design data recording medium on which  
2 design data for forming an integrated circuit on a  
3 semiconductor chip is recorded so as to be readable by a  
4 computer, the design data comprising:

5 first mask pattern data for determining a figure  
6 pattern for forming a well region on which a plurality of  
7 logic gates is formed,



8 second mask pattern data for determining a figure  
9 pattern for forming a first line pair, a second line pair  
10 and a third line pair on said well region, and  
11 third mask pattern data for determining a figure  
12 pattern for forming a plurality of connectors,  
13 wherein a first group of said connectors connects said  
14 first line pair and portions of said well region,  
15 wherein a second group of said connectors connects  
16 said second line pair and a first group of said logic gates  
17 for supplying said first group of logic gates with a first  
18 potential difference as a sole operation power source from  
19 said second line pair, and  
20 wherein a third group of said connectors connects said  
21 third line pair and a second group of said logic gates for  
22 supplying said second group of logic gates with a second  
23 potential difference, which is larger than said first  
24 potential difference, as a sole operation power source from  
25 said third line pair.

1 58. (New) A design data recording medium on which  
2 design data for designing an integrated circuit to be  
3 formed on a semiconductor chip is recorded so as to be  
4 readable by a computer, the design data comprising:

5 first function description data for determining a  
6 function of a first logic gate which is supplied with a  
7 first potential difference as a sole operation power source  
8 from a first pair of potential lines and a substrate  
9 potential from a substrate potential line;

10 second function description data for determining a  
11 function of a second logic gate which is supplied with a  
12 second potential difference as a sole operation power  
13 source from a second pair of potential lines and a  
14 substrate potential from said substrate potential line; and

15 third function description data for determining said  
16 first potential difference to be smaller than said second  
17 potential difference.

1 59. (New) A design data recording medium according to  
2 claim 58,

3 wherein said well region includes a first well portion  
4 and a second well portion,

5 wherein said first mask pattern data includes fourth  
6 mask pattern data and fifth mask pattern data,

7 wherein said fourth mask pattern data is for  
8 determining a figure pattern for forming the first well  
9 portion, and

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10 wherein said fifth mask pattern data is for  
11 determining a figure pattern for forming the second well  
12 portion.

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